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FULLY-DEPLETED (FD) (SOI) MOSFET ACCESS TRANSISTOR AND METHOD  
OF FABRICATION

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# **FULLY-DEPLETED (FD) (SOI) MOSFET ACCESS TRANSISTOR AND METHOD OF FABRICATION**

## **FIELD OF THE INVENTION**

[0001] The present invention relates to the field of semiconductor integrated circuits and, in particular, to Silicon-on-Insulator (SOI) devices.

## **BACKGROUND OF THE INVENTION**

[0002] Silicon-on-Insulator (SOI) technology employs a layer of semiconductor material formed over an insulating layer on a supporting bulk wafer. The structure can be formed by different well-known techniques in the art, for example, separation by implanted oxygen (SIMOX), bonding and etching back (BESOI), and zone melting and recrystallization (ZMR), among others. Typically, the structure comprises a film of monocrystalline silicon formed on a buried layer of silicon dioxide which is formed on a monocrystalline silicon substrate.

[0003] One technique for the formation of a SOI substrate by a conventional bonding and etching back method of the prior art is illustrated in Figures 1-4. The process starts with the preparation of a silicon substrate 10 (Figure 1). The silicon substrate 10 is thermally oxidized to grow a layer of silicon oxide 12 (Figure 1), with a thickness of about 1,000 Å to about 2 μm. Subsequently, a single crystalline silicon substrate 14 is opposed to the silicon oxide layer 12, as shown in Figure 2. The silicon substrate 10, with the oxide layer 12, is then contacted with the crystalline silicon substrate 14, and the resultant structure is heated to a temperature of about 1000°C, so

that the crystalline silicon of the crystalline silicon substrate 14 adheres to the silicon oxide layer 12, as shown in Figure 3. Next, as illustrated in Figure 4, the crystalline silicon substrate 14 is polished and its thickness is decreased to approximately 1.5 microns. Thus, a SOI substrate 15 (Figure 4) is formed of the silicon substrate 10, the silicon oxide layer 12, and the crystalline silicon substrate 14.

[0004] Field effect transistors such as MOSFETs, which are fabricated in the upper silicon layer of a SOI structure, such as the SOI substrate 15 of Figure 4, are known in the art. Typically, MOSFETs are fabricated by placing an undoped polycrystalline material, for example polysilicon, over a relatively thin gate oxide, and implanting the polycrystalline material and adjacent active regions with an impurity dopant material to form source and drain regions. If the impurity dopant material for forming the source/drain regions is n-type, then the resulting MOSFET is an NMOSFET (“NMOS”) device. Conversely, if the impurity dopant material for forming the source/drain regions is p-type, then the resulting MOSFET is a PMOSFET (“PMOS”) device.

[0005] Field effect transistors fabricated in the upper silicon layer of a SOI structure, such as the SOI substrate 15 of Figure 4, have multiple advantages over the transistors fabricated on the conventional bulk silicon substrates. These advantages include, among others, resistance to short-channel effect, increased current drive, higher packing density, and reduced parasitic capacitance. However, despite all these attractive properties, SOI technology still has some drawbacks, which reduce the benefits of using it for high-performance and high-density ultra large scale integrated (ULSI) circuits.

[0006] One drawback of the SOI technology is the conductivity of the top silicon layer and its inherent floating body effect, which has particular significance for partially-depleted (PD) or non-fully depleted SOI devices. The floating body effect in such devices occurs as a result of the buried oxide that isolates the channel region of such device and allows charge carriers to build up in the channel region. In a partially-depleted MOSFET, charge carriers (holes in an nMOSFET and electrons in a pMOSFET), generated by impact ionization and drain junction leakage near the drain/body region, accumulate near the source/body region of the transistor. When sufficient carriers accumulate, they are stored in the floating body, which is formed right below the channel region, and alter the floating body potential. As a result, kinks in the I/V curve occur, the threshold voltage is lowered, the dynamic data retention time is altered, and the overall electrical performance of the device may be severely degraded.

[0007] One technique for diminishing the negative effects of the charge build up has been to provide an extra electrical connection by adding a contact to the body for hole current collection. However, the currently available hole collection schemes, such as the use of a side-contact, are inefficient, require very complex processing steps, and consume a great amount of device area.

[0008] Another technique for diminishing the negative effects of the charge build up has been to use a fully depleted (FD) SOI MOSFET. For this, the silicon layer or island must be sufficiently thin, less than about 400 Angstroms for state-of-the art technology, so that the entire thickness of the body region is depleted of majority carriers and both junctions are at ground. Unfortunately, silicon islands of less than 400 Angstroms thick are extremely costly and difficult to manufacture, due

primarily to the sensitivity to variations of silicon film thickness and doping profile across the wafer, as well as to the large source/drain parasitic resistance. In addition, the low threshold voltage ( $V_T$ ) of a conventional fully depleted (FD) SOI causes large subthreshold leakage and low subthreshold voltage ( $V_t$ ), which in turn greatly reduce the static retention time of a DRAM.

[0009] Accordingly, there is a need for an improved method for forming a fully-depleted SOI device having reduced charge build up and accompanying threshold voltage changes and charge leakage. There is also a need for an integrated memory process for SOI wafer fabrication in which access transistors are created with fewer processing steps and which saves wafer area. A defect-free fully-depleted SOI device which is highly immune to soft errors (due to alpha particles and cosmic ray irradiation) is also needed.

### SUMMARY OF THE INVENTION

[0010] The present invention provides a fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET device, for example, a FD SOI NMOS access transistor, with high threshold voltage and reduced leakage. The present invention also provides a simple method for forming a fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET device on a SOI substrate, which does not require an additional silicon thinning process which is typical for the formation of such fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET devices.

[0011] The fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET device of the present invention comprises a gate electrode of a conductivity type which

is opposite the conductivity type of the source/drain regions. For example, a FD SOI NMOS access transistor formed in the memory array area of a SOI substrate according to the present invention comprises a p+ gate electrode and n+ source and drain regions. The p+ gate electrode ensures the fully-depleted working mode of the SOI NMOS device.

[0012] The present invention also provides at least one fully-depleted (FD) SOI MOSFET device of a first conductivity type in a memory array area of a SOI substrate, and at least one partially-depleted (PD) SOI MOSFET device of the same conductivity type in a periphery area of the SOI substrate. The fully-depleted (FD) SOI MOSFET device of the first conductivity type comprises a gate electrode of a second conductivity type which reduces the charge build up and the leakage current.

[0013] The present invention further provides a method of forming at least one partially-depleted (PD) SOI MOSFET device of a first conductivity type in a periphery area of a SOI substrate, while at least one fully-depleted (FD) SOI MOSFET device of the first conductivity type is formed in a memory array area of the SOI substrate. According to the present invention, the gate electrode of the fully-depleted (FD) SOI MOSFET device of the first conductivity type formed in the memory array area is doped with dopants of a second conductivity type to guarantee the fully-depleted working mode for the access SOI MOSFET in the memory array area. The fully-depleted (FD) SOI MOSFET device of the present invention is fabricated on a SOI substrate which does not have to undergo an extra a silicon thinning process which is typically required for the formation of such fully-depleted (FD) SOI MOSFET devices.

[0014] The above and other advantages and features of the present invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 is a cross-sectional view of a SOI substrate at an initial stage of processing and in accordance with a method of the prior art.

[0016] Figure 2 is a cross-sectional view of the SOI substrate of Figure 1 at a stage of processing subsequent to that shown in Figure 1.

[0017] Figure 3 is a cross-sectional view of the SOI substrate of Figure 1 at a stage of processing subsequent to that shown in Figure 2.

[0018] Figure 4 is a cross-sectional view of the SOI substrate of Figure 1 at a stage of processing subsequent to that shown in Figure 3.

[0019] Figure 5 is a cross-sectional view of a portion of a SOI substrate at an initial stage of processing on which a PD SOI NMOS device and a FD SOI NMOS device will be fabricated in accordance with an embodiment of the present invention.

[0020] Figure 6 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 5.

[0021] Figure 7 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 6.

[0022] Figure 8 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 7.

[0023] Figure 9 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 8.

[0024] Figure 10 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 9.

[0025] Figure 11 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 10.

[0026] Figure 12 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 11.

[0027] Figure 13 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 12.

[0028] Figure 14 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 13.

[0029] Figure 15 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 14.

[0030] Figure 16 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 15.

[0031] Figure 17 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 16.

[0032] Figure 18 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 17.

[0033] Figure 19 is a cross-sectional view of the SOI substrate of Figure 5 at a stage of processing subsequent to that shown in Figure 18.

[0034] Figure 20 illustrates schematically the partially-depleted and fully-depleted modes of the two NMOS devices of Figure 19.

[0035] Figure 21 is a graph illustrating the dependency of the drain current vs. gate voltage for a p+ gate FD SOI NMOS transistor fabricated according to an embodiment of the present invention.



[0036] Figure 22 is a simulated comparative graph illustrating the change of the threshold voltage vs. the change of silicon film thickness for an n+ gate FD SOI NMOS transistor of the prior art and a p+ gate FD SOI NMOS transistor fabricated of the present invention.

[0037] Figure 23 is a cross-sectional view of a DRAM memory device fabricated on the SOI substrate of Figure 5 and comprising at least one FD SOI NMOS device fabricated in accordance with the present invention.

[0038] Figure 24 is an illustration of a processing system having a memory cell access transistor comprising a MOSFET device constructed on a SOI substrate according to the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039] In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that various structural, logical, and electrical changes may be made without departing from the spirit or scope of the invention.

[0040] The present invention provides a method of forming at least one partially-depleted (PD) SOI MOSFET device of a first conductivity type in a periphery area of a SOI substrate, while at least one fully-depleted (FD) SOI MOSFET device of the first conductivity type is formed in a memory array area of the SOI substrate.

According to the present invention, the gate electrode of the fully-depleted (FD) SOI MOSFET device of the first conductivity type formed in the memory array area is doped with impurity atoms of a second conductivity type to guarantee the fully-depleted working mode for the access SOI MOSFET in the memory array area. This way, the fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET device of the present invention has reduced leakage without reducing the threshold voltage, and is fabricated without extra thinning of silicon, which is typically required for the formation of such fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFET devices.

[0041] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 5-19 illustrate a method for the fabrication of both a partially-depleted (PD) SOI MOSFET 200 (Figure 19) and a fully-depleted (FD) SOI MOSFET 100 (Figure 19) of the same conductivity type and on the same silicon film. As described in detail below, the partially-depleted (PD) NMOS transistor 200 (Figure 19) and the fully-depleted (FD) SOI NMOS transistor 100 (Figure 19) comprising a p+ gate electrode 60a (Figures 17-19) are both formed on the same SOI substrate 40. Thus, the present invention eliminates the need for an extra silicon thinning process conventionally employed in the formation of a fully-depleted (FD) SOI MOSFET.

[0042] Although the present invention will be described below with reference to the formation of two NMOS transistors each in their respective periphery and memory array regions of a SOI substrate, such as the partially-depleted (PD) NMOS transistor 200 (Figure 19) and the fully-depleted (FD) SOI NMOS transistor 100 (Figure 19), it must be understood that the invention is not limited to this embodiment. Accordingly, the invention also contemplates the formation of PMOS

transistors in both the periphery and memory access regions, as well as the formation of a plurality of fully-depleted (FD) and partially-depleted (PD) transistors of the same or different conductivity type. In addition, although the partially-depleted (PD) NMOS transistor 200 (Figure 19) and the fully-depleted (FD) SOI NMOS transistor 100 (Figure 19) are illustrated as being adjacent in the drawings, in actual practice this will likely not occur, as FD SOI NMOS transistor 100 is formed in a memory array area of a memory device and PD SOI NMOS transistor 200 is formed in a peripheral logic area outside the memory array area. Thus, the below illustrated and described embodiments are only exemplary, and the present invention is not limited to the illustrated embodiments.

[0043] Figure 5 illustrates a silicon-on-insulator (SOI) substrate 40 formed, for example, by a SIMOX, BESOI or ZMR technique. The SOI substrate 40 comprises a first silicon substrate 50 and an insulating layer 52, for example, a buried silicon oxide insulating layer 52. The SOI substrate 40 of Figure 5 also comprises a second silicon substrate 54.

[0044] Although reference to the thermally grown insulating layer 52 (Figure 5) will be made in this application as to the silicon dioxide layer 52 or the buried silicon oxide layer 52, it must be understood that the present invention has applicability to other types of thermally grown insulating oxides. Thus, the present invention is not limited to silicon oxides, and other oxides, such as oxynitrides and sapphire-intermediate oxides grown by chemical vapor deposition (CVD), may be used also in accordance with the characteristics of the particular SOI device. Similarly, although the present invention is explained with reference to silicon substrates, such as

the first and second silicon substrates 50, 54 (Figure 5), it must be understood that the substrate need not be silicon-based. Thus, the invention has equal applicability to other semiconductor substrates, such as, for example, silicon-germanium, germanium, silicon-on-sapphire, or gallium-arsenide substrates.

[0045] Referring now to Figure 6, the thickness of the second silicon substrate 54 is reduced by thermal oxidation, for example, to achieve a thin silicon layer 55 of about 200 Angstroms to about 1,500 Angstroms, more preferably of about 300 Angstroms to about 1,200 Angstroms. During the thermal oxidation process, the top surface (not shown) of the silicon material of the second silicon substrate 54 is oxidized to form a silicon oxide layer (not shown) which is subsequently removed, by wet etch for example, to form the thin silicon layer 55 (Figure 6).

[0046] According to the present invention and as explained in more detail below, the thin silicon layer 55 need not have a thickness less than about 500 Angstroms, which is required for the body region to be fully depleted of majority carriers when the SOI MOSFET device is in the "on" state and both junctions are at ground. Thus, in the embodiments described below, fully-depleted SOI MOSFET devices will be formed without an extra (or additional) silicon thinning process, that is, without further reducing the thickness of the silicon layer 55, which is of about 500 Angstroms to about 1,500 Angstroms, to less than about 500 Angstroms.

[0047] Subsequent to the thinning process of the second silicon substrate 54 and the formation of the thin silicon layer 55 (Figure 6), an isolation region 51 (Figure 7) is formed in the thin silicon layer 55 by any known technique, such as

thermal oxidation of the underlying silicon in a LOCOS process, or by etching trenches and filling them with a dielectric or an oxide material in an STI process. This way, the isolation region 51 (Figure 7) may be a field oxide region (FOX) or a shallow trench for isolation (STI).

[0048] According to an exemplary embodiment of the present invention, the isolation region 51 (Figure 5) is a shallow trench for isolation filled with high density plasma (HDP) oxide, a material which has a high ability to effectively fill narrow trenches. Alternatively, an insulating layer (not shown) formed of an oxide or of silicon nitride, for example, may be formed on the trench sidewalls, prior to filling the trench with the isolation dielectric, to aid in smoothing out the corners in the bottom of the trench and to reduce the amount of stress in the dielectric used to later fill in the trench.

[0049] As known in the art, the isolation region 51 provides electrical and physical separation, as well as isolation between neighboring transistor regions on the SOI substrate 40. As illustrated in Figure 7, the isolation region 51 isolates region A of the thin silicon layer 55 on which memory access circuitry will be subsequently formed, from region B of the thin silicon layer 55 on which peripheral circuitry will be subsequently formed, all according to embodiments of the present invention.

[0050] Subsequent to the formation of the isolation region 51 (Figure 7), a thin gate oxide layer 56, which will act as a gate insulator layer, is formed over the thin silicon layer 55, as shown in Figure 8. The thin gate oxide layer 56 may comprise silicon dioxide ( $\text{SiO}_2$ ), for example, which may be thermally grown in an oxygen ambient, at a temperature between about 600°C to about 1000°C and to a thickness of

about 10 Angstroms to about 100 Angstroms. The gate insulator is not limited to silicon oxide and other dielectric materials such as oxynitride,  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$  or other high k material may be used as gate insulator layer.

[0051] As illustrated in Figure 9, an undoped gate layer 58 is formed over the thin gate oxide layer 56. According to an embodiment of the present invention, the undoped gate layer 58 is formed of polysilicon which may be deposited over the thin gate oxide layer 56 by, for example, a low plasma chemical vapor deposition (LPCVD) method at a temperature of about 300°C to about 700°C and to a thickness of about 100 Angstroms to about 2,000 Angstroms.

[0052] According to another embodiment of the present invention, the undoped gate layer 58 is a layer of silicon/germanium (Si/Ge) material. According to this embodiment, the gate silicon/germanium layer 58 is grown by a low plasma chemical vapor deposition (LPCVD) method in a reaction chamber at a temperature of about 900°C to about 1200°C, and by employing a silicon (Si) and germanium (Ge) gas source to introduce a gaseous species containing silicon and germanium in the same reaction chamber.

[0053] The silicon gas source may be, for example, silane ( $\text{SiH}_4$ ), higher order silanes, such as disilane ( $\text{Si}_2\text{H}_6$ ), as well as other gaseous sources of silicon, such as dichlorsilane ( $\text{SiH}_2\text{Cl}_2$ ), trichlorsilane ( $\text{SiHCl}_3$ ), or tetrachlorsilane ( $\text{SiCl}_4$ ). The germanium gas source may be, for example, a germane ( $\text{GeH}_4$ ) source, or any other gaseous source containing germanium. The combination of the two gaseous sources allows deposition of the gate silicon/germanium layer 58 to a thickness of about 100

Angstroms to about 1500 Angstroms, more preferably of about 500 Angstroms to about 900 Angstroms. The gate silicon/germanium layer 58 has a germanium composition of approximately 0-100% of the total composition, more preferably of about 15-50%. The thickness of the gate silicon/germanium layer 58 is proportional to, and depends upon, the deposition time. Although, as described above, the undoped gate layer 58 may be formed of various materials, reference to the undoped gate layer 58 will be made in this application as to the undoped polysilicon layer 58. However, the invention also encompasses embodiments with a metal gate, for example, TiN, Ti, Ni, Mo and TaNx among others, with appropriate work functions and which can be used similarly to the N/P+ poly gate approach.

[0054] Subsequent to the formation of the undoped polysilicon layer 58 (Figure 9), a first patterned photoresist layer 59a (Figure 10) is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms over the undoped polysilicon layer 58 and the region A, but not over the region B on which periphery circuitry will be subsequently formed according to a method of the present invention. Thus, using the thick patterned photoresist layer 59a as a mask, dopant or impurity atoms of a first conductivity type are introduced into the exposed portion of the undoped polysilicon layer 58 located above the region B of the SOI substrate 40 by using a first ion implantation 61 (Figure 10) to form a doped polysilicon layer 60b, illustrated in Figure 11.

[0055] According to an exemplary embodiment of the invention, the dopant or impurity atoms of the first conductivity type are of n-type conductivity for NMOS device fabrication. Thus, n-type dopants such as phosphorous (P), arsenic (As)

or antimony (Sb) are implanted into the exposed region of the undoped polysilicon layer 58 by using the first ion implantation 61 (Figure 10) to form the n+ doped polysilicon layer 60b (Figure 11). Ion implantation is performed by placing the SOI substrate 40 in an ion implanter, for example, and implanting appropriate dopant ions into the exposed portion of the undoped polysilicon layer 58. For example, phosphorous is introduced into the exposed portion of the undoped polysilicon layer 58 of Figure 10 using ion implantation at an accelerated energy of about 1keV to about 50keV and a dose concentration of about  $1 \times 10^{15}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ . A heat treatment such as an anneal treatment at about 600°C to about 1000°C, may be optionally employed to activate the dopant within the n+ doped polysilicon layer 60b of Figure 11.

[0056] Subsequent to the formation of the n+ polysilicon layer 60b of Figure 11, the SOI substrate 40 undergoes a second ion implantation 63 (Figure 11) using the first patterned photoresist layer 59a as a mask, this time with dopant impurity ions of a second conductivity type. In this manner, p-type dopant impurity ions, such as boron (B), boron fluoride ( $\text{BF}_2$ ) or indium (In) are implanted into the thin silicon layer 55 to form a p-type well 62b as shown in Figure 12. Ion implantation is performed by placing the SOI substrate 40 in an ion implanter, for example, and implanting appropriate p-type dopant ions into the thin silicon layer 55 located above the region B of the SOI substrate 40. For example, boron is introduced into the thin silicon layer 55 of Figure 11 using ion implantation at an accelerated energy of about 15keV to about 150keV and a dose concentration of about  $1 \times 10^{11}/\text{cm}^2$  to about  $5 \times 10^{13}/\text{cm}^2$ . A heat treatment, for example, an anneal treatment at about 600°C to about 1000°C, may be optionally employed to activate the dopant within the doped p well 62b of Figure 12.



[0057] Although the invention has been described above with reference to the formation of the p well 62b (Figure 12) subsequent to the formation of the n+ polysilicon layer 60b (Figure 11), the invention is not limited to this exemplary embodiment. As such, the invention also contemplates the formation of the p well 62b first, and then followed by the formation of the n+ polysilicon layer 60b.

[0058] Referring now to Figure 13, a second patterned photoresist layer 59b is formed to a thickness of about 1,000 Angstroms to about 10,000 Angstroms over the n+ doped polysilicon layer 60b and the p doped well 62b, but not over the region A on which memory access circuitry will be subsequently formed according to a method of the present invention. Accordingly, using the thick patterned photoresist layer 59b as a mask, dopant or impurity atoms of the second conductivity type are introduced into the exposed portion of the undoped polysilicon layer 58 located above the region A of the SOI substrate 40 to form a p+ doped polysilicon layer 60a, as illustrated in Figure 14.

[0059] P-type dopant impurity ions, such as boron (B), boron fluoride ( $\text{BF}_2$ ) or indium (In) are implanted into the exposed region of the undoped polysilicon layer 58 of Figure 13 by using a third ion implantation 65 (Figure 13) to form the p+ doped polysilicon layer 60a (Figure 14). Ion implantation is performed by placing the SOI substrate 40 in an ion implanter, and implanting appropriate dopant ions into the exposed portion of the undoped polysilicon layer 58. For example, boron is introduced into the exposed portion of the undoped polysilicon layer 58 of Figure 13 using ion implantation at an accelerated energy of about 1keV to about 50keV and a dose

concentration of about  $1 \times 10^{15}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ . A heat treatment, for example, an anneal treatment at about  $600^\circ\text{C}$  to about  $1000^\circ\text{C}$ , may be optionally employed to activate the dopant within the p+ doped polysilicon layer 60a of Figure 14.

[0060] According to an embodiment of the invention and subsequent to the formation of the p+ polysilicon layer 60a of Figure 14, the SOI substrate 40 may optionally undergo a fourth ion implantation 67 (Figure 14) to form a lightly doped or very lightly doped p-type well 62a illustrated in Figure 15. For the purposes of the present invention, "light doping" is defined as doping with a dose concentration of about  $1 \times 10^9/\text{cm}^2$  to  $1 \times 10^{12}/\text{cm}^2$ , more preferably of about  $1 \times 10^{10}/\text{cm}^2$  to  $5 \times 10^{11}/\text{cm}^2$ . Lightly doping the thin silicon layer 55 to form the p-type well 62a of the SOI substrate 40 is optional, as the p+ polysilicon layer 60a (which will form p+ gate electrode 60a of Figure 17) has a large workfunction and can confer a threshold voltage of about 1.0V even without the lightly doping of the silicon layer.

[0061] In an exemplary embodiment of the invention, the thin silicon layer 55 corresponding to the region A of the SOI substrate 40 undergoes a light doping using the second patterned photoresist layer 59b as a mask, with dopant impurity ions of the second conductivity type. In this manner, p-type dopant impurity ions, such as boron (B), boron fluoride ( $\text{BF}_2$ ) or indium (In) are implanted into the thin silicon layer 55 corresponding to region A (Figure 14) to form a lightly-doped p-type well 62a as shown in Figure 15.

[0062] Ion implantation is performed by placing the SOI substrate 40 in an ion implanter, for example, and implanting appropriate light doses of p-type dopant

ions into the thin silicon layer 55 corresponding to the region A of the SOI substrate 40. For example, boron is introduced into the thin silicon layer 55 of Figure 14 using ion implantation at an accelerated energy of about 1keV to about 60keV and a light dose concentration of about  $1 \times 10^{11}/\text{cm}^2$ . A heat treatment, for example, an anneal treatment at about 600°C to about 1000°C, may be optionally employed to activate the dopant within the lightly-doped p+ well 62a of Figure 15.

[0063] Although the invention has been described above with reference to the formation of the p well 62a (Figure 15) subsequent to the formation of the p+ polysilicon layer 60a (Figure 14), the invention is not limited to this exemplary embodiment. As such, the invention also contemplates the formation of the p well 62a first, and then followed by the formation of the p+ polysilicon layer 60a.

[0064] Referring now to Figure 16 and in accordance with an exemplary embodiment of the present invention, silicide regions 64 may be formed over the doped polysilicon layers 60a, 60b (Figure 15). If the silicide regions are desired, a layer of metal capable of forming a silicide may be deposited over the doped polysilicon layers 60a, 60b (Figure 15) by sputtering by RF or DC or by other similar methods such as CVD, to a thickness of about 100 Angstroms to about 800 Angstroms. Subsequent to the deposition of the metal capable of forming a silicide, the SOI substrate 40 undergoes a rapid thermal anneal (RTA), typically for about 10 to 60 seconds, using a nitrogen ambient at about 600°C to about 850°C, so that the metal in direct contact with the doped polysilicon layers 60a, 60b is converted to its silicide. As shown in Figure 16, silicide regions 64 form conductive regions on top of the doped polysilicon layers 60a, 60b. Preferably, the refractory metal has low resistance and low resistivity as

a silicide. However, the refractory metal silicide may comprise any refractory metal, including but not limiting to titanium, cobalt, tungsten, tantalum, molybdenum, and platinum.

[0065] Although the following processing steps for the completion of the gate stacks 70a, 70b (Figure 17) will refer to and illustrate the silicide regions 64 formed over the doped polysilicon layers 60a, 60b, it must be understood that the present invention is not limited to this embodiment, and other embodiments such as the formation of gate stacks without a silicide layer on the polysilicon gate, are also contemplated. In any event, a cap material 65 is formed over the silicide regions 64, as also illustrated in Figure 16. The cap material may be formed of silicon dielectrics such as silicon nitride or silicon oxide, but TEOS or carbides may be used also. The cap material 60 may be formed via PECVD and LPCVD deposition procedures, for example, at a temperature between about 300°C to about 1000°C, to a thickness of about 500 Angstroms to about 2,000 Angstroms.

[0066] Next, the structure of Figure 16 is patterned with a photoresist layer and a mask which are both formed over the cap material 65. In this manner, the doped polysilicon layers 60a, 60b, the optional silicide region 64 and the cap material 65 are anisotropically etched through the patterned photoresist, to obtain a plurality of polysilicon gates 70a, 70b, illustrated in Figure 17. Each of the gate stacks 70a, 70b comprises a polysilicon layer, the optional silicide region 64 and the nitride cap 65. Gate 70b comprises the n+ doped polysilicon layer 60b, while gate 70a comprises the p+ doped polysilicon layer 60a.

[0067] The gate stacks 70a, 70b may now be used in a self-aligned implant process where the gate stacks mask the dopant implantation of source/drain regions 73a, 73b (Figure 19) of the adjacent transistors defined by the gate stacks. As such, Figure 18 illustrates the formation of lightly doped drain (LDD) regions 71a, 71b in the SOI substrate 40. As known in the art, the LDD regions 71a, 71b may be formed by implanting low dosages of conductivity-altering dopants with an LDD mask (not shown) and using the gate stacks 70a, 70b as an implantation mask. Thus, in the p well 62a of the region A of the SOI substrate 40, n-type dopants such as arsenic or phosphorous may be implanted at a low energy dose, for example of about  $2 \times 10^{14}$  atoms/cm<sup>2</sup>, using the gate stack 70a as a mask. Similarly, in the p well 62b of the region B of the SOI substrate 40, n-type dopants such as arsenic or phosphorous may be also implanted at a low energy dose, for example of about  $2 \times 10^{14}$  atoms/cm<sup>2</sup>, using the gate stack 70b as a mask.

[0068] The next step in the process flow is the formation of spacers 74 illustrated in Figure 19. Spacers 74 may be formed, for example, by blanket depositing a silicon nitride film or a silicon oxide material over the structure of Figure 18 and then anisotropically etching it with an RIE plasma to form the spacers 74 on each of the sidewalls of the gate stacks 70a, 70b.

[0069] The gate stacks 70a, 70b protected by spacers 74 can now undergo processing steps for the formation of source/drain regions in the SOI substrate 40. As such, using the gate stacks 70a, 70b as an implantation mask, heavily doped source/drain regions 73a, 73b are formed in the uncovered portions of the SOI substrate 40 via an ion implantation procedure performed at an energy of about 3KeV

to about 50keV, and at a dose of about  $1 \times 10^{15}$  to about  $5 \times 10^{15}$  atoms/cm<sup>2</sup>, using an n-type dopant such as arsenic or phosphorous, for example. Thermal annealing for activation may be carried out in a nitrogen atmosphere at about 850°C to about 1050°C and for about 10 seconds to about 10 minutes.

[0070] This way, source and drain regions 73a, 73b (Figure 19), which are heavily doped with n-type impurity ions, are formed within the p-type wells 62a, 62b. Thus, two n-p-n type (NMOS) transistors 100, 200 (Figure 19) are formed of the gate stacks 70a, 70b and their respective n-type source/drain regions 73a, 73b within the p-type wells 62a, 62b. As explained in more detail below and with reference to Figure 20, the first NMOS transistor 100 formed in the memory array area is a fully-depleted (FD) SOI NMOS transistor with a p+ gate electrode, as opposed to a conventional n+ gate electrode. The p+ gate electrode with low channel doping ensures the fully-depleted mode for the access SOI NMOS transistor 100 in the memory array. The second NMOS transistor 200 formed in the periphery area is a partially-depleted, and not fully-depleted, SOI NMOS transistor. Thus, a fully-depleted and a partially-depleted MOSFET devices of the same conductivity type are formed on the same SOI substrate and without the conventional silicon thinning of the silicon layer of the prior art to obtain a fully-depleted device.

[0071] Figure 20 illustrates schematically the depletion regions in the fully-depleted (FD) SOI NMOS transistor 100 having a p+ gate electrode and the partially-depleted (PD) SOI NMOS transistor 200 formed on the same SOI substrate. The partially-depleted (PD) SOI NMOS transistor 200 of Figure 20 is called “partially-depleted” because depletion region 75b (Figure 20) does not touch the buried oxide

layer 52. Instead, neutral floating body region 77 of the partially-depleted (PD) SOI NMOS transistor 200 is interposed between the depletion region 75b and two junction regions 76b (Figure 20). In contrast, the fully-depleted (FD) SOI NMOS transistor 100 comprising a p+ gate electrode fabricated according to the present invention is called “fully-depleted” because depletion region 75a (Figure 20) touches the buried oxide layer 52. Thus, as illustrated in Figure 20, no neutral floating body region is interposed between the depletion region 75a and junction regions 76a (Figure 20) of the fully-depleted (FD) SOI NMOS transistor 100. This is because the existence of the p+ doped polysilicon gate electrode 60a and the very low channel doping concentration confer a much larger depletion depth than the thickness of the silicon layer 62a.

[0072] Examples of the implementation of the present invention and of the characteristics of the p+ gate FD SOI NMOS transistor fabricated according to the present invention will now be described with reference to Figures 21-22.

[0073] Figure 21 illustrates the dependency of the drain current ( $I_d$ ) versus the gate voltage ( $V_g$ ) for a p+ gate fully-depleted (FD) SOI NMOS transistor fabricated according to an embodiment of the present invention. The p+ gate FD SOI NMOS transistor was fabricated on a SOI substrate comprising a buried oxide layer with a thickness of about 3600 Angstroms and an upper silicon layer with a thickness of about 634 Angstroms. The gate stack of the p+ gate FD SOI NMOS transistor comprised a thin gate oxide layer of about 47 Angstroms thick and a p+ doped polysilicon layer of about 750 Angstroms thick. The p+ doped polysilicon layer had a boron dopant concentration of about  $3 \times 10^{15}/\text{cm}^2$ . After the formation of the p+ doped polysilicon layer, the p+ gate FD SOI NMOS transistor underwent no p-well formation,

as the channel doping concentration was equal to the intrinsic substrate concentration, of about  $1 \times 10^{15}/\text{cm}^3$ .

[0074] Measurements for the drain current and gate voltage were conducted on the p+ gate FD SOI NMOS transistor described above for a  $V_{ds}$  (drain/source voltage) of about 0.05V. Data from the measurements was recorded and illustrated in Figure 21. The distribution of the drain current ( $I_d$ ) as function of the gate voltage ( $V_g$ ) of Figure 21 demonstrates that the  $I_d/V_g$  curve of the p+ gate FD SOI NMOS transistor of the present invention is similar to that of an n+ gate FD SOI NMOS transistor of the prior art.

[0075] For example, region A of Figure 21 corresponds to gate voltage values in the range of about  $-0.5\text{V}$  to about  $0.3\text{V}$  and drain current values in the range of about  $10^{-15}\text{A}$  to about  $10^{-13}\text{A}$ . For drain current and gate voltage values falling in the region A of Figure 21, the p+ gate FD SOI NMOS transistor is in the “off” state. Similarly, region B of Figure 21 corresponds to gate voltage values in the range of about  $0.3\text{V}$  to about  $1.0\text{V}$  and drain current values in the range of about  $10^{-13}\text{A}$  to about  $10^{-5}\text{A}$ . For drain current and gate voltage values falling in the region B of Figure 21, the p+ gate FD SOI NMOS transistor begins to turn “on” and enters the subthreshold mode. As shown in Figure 21, the drain current of the p+ gate FD SOI NMOS transistor increases as the gate voltage increases. Finally, region C of Figure 21 corresponds to gate voltage values in the range of about  $1.0\text{V}$  to about  $2.5\text{V}$  and drain current values of about  $10^{-4}\text{A}$ . For drain current and gate voltage values falling in the region C of Figure 21, the p+ gate FD SOI NMOS transistor is totally turned “on.” As



shown in Figure 21, the drain current of the p+ gate FD SOI NMOS transistor increases as the gate voltage increases.

[0076] The measurements recorded in Figure 21 demonstrate that the  $I_d/V_g$  curve of the p+ gate FD SOI NMOS transistor fabricated according to an embodiment of the present invention follows the characteristics of an  $I_d/V_g$  curve of an n+ gate FD SOI NMOS transistor of the prior art. Thus, good performance characteristics have been obtained for the p+ gate FD SOI NMOS transistor of the present invention without decreasing the thickness of the upper silicon layer of the SOI substrate and reducing threshold voltage.

[0077] Figure 22 is a simulated graph of the change in the threshold voltage ( $\Delta V_{th}$ ) vs. change in the silicon thickness ( $\Delta T_{si}$ ) for 2 different NMOS transistors: a simulated n+ gate SOI NMOS transistor of the prior art (reference transistor) and a simulated p+ gate SOI NMOS transistor of the present invention. The simulation data was collected and gathered by a transistor simulator SILVACO. For the simulated n+ gate SOI NMOS transistor, the reference silicon film thickness was of about 25nm at a reference threshold voltage of about 0.171V. For the simulated p+ gate SOI NMOS transistor, the reference silicon film thickness was of about 65nm at a reference threshold voltage of about 0.90307V.

[0078] As known in the art, the threshold voltage of a SOI MOSFET device depends on changes in the silicon film thickness. Since the fully-depleted SOI NMOS transistor of the prior art requires a much thinner silicon film than the partially-depleted SOI NMOS transistor, the thickness of the silicon film varies across a wafer

comprising a partially-depleted and a fully-depleted transistors. This change in the silicon film thickness causes, in turn, great threshold voltage variations. Accordingly, the characteristics of the fully-depleted SOI MOSFET devices of the prior art are greatly and undesirably impacted by the variations in the silicon film thickness.

[0079] Figure 22 demonstrates that the threshold voltage of the simulated p+ gate SOI NMOS transistor of the present invention remains constant with the change in the silicon film thickness. Thus, the simulated p+ gate SOI NMOS transistor of the present invention is not vulnerable to variations in the silicon film thickness across the wafer. In contrast, the threshold voltage of the simulated n+ gate SOI NMOS transistor undesirably increases with the change in the silicon film thickness. The collected data demonstrates that the p+ gate SOI FD NMOS transistor is more manufacturable than the n+ gate SOI FD NMOS transistor because the characteristics of the p+ gate SOI NMOS transistor are not vulnerable to process variations.

[0080] The FD SOI NMOS transistor 100 (Figures 19-20) may be used as an access transistor in a memory device such as a random access memory device. For example, Figure 23 illustrates a portion of a memory array area of the SOI substrate 40 on which a DRAM memory device 300 is formed in accordance with embodiments of the present invention.

[0081] As illustrated in Figure 23, the DRAM memory device 300 is formed of a pair of memory cells comprising respective access FD SOI NMOS transistors, at least one being a p+ gate FD SOI NMOS transistor 100 formed according to the present invention. Figure 23 depicts conductors 89 and capacitors 99 with

associated conductive plugs 99a, all formed within one or more insulating layers, such as insulating layer 97, formed over the access FD SOI NMOS transistors 100.

[0082] The DRAM memory device 300 (Figure 23) containing at least one fully-depleted (FD) SOI NMOS transistor 100 (Figure 19), either by itself or in combination with the partially-depleted (PD) SOI NMOS transistor 200, may now be employed in any integrated circuit structures, for example, in a processing system such as the one illustrated in Figure 24. The exemplary processing system 900 of Figure 24 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0083] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one p+ gate FD SOI NMOS device 100 of the present invention, either by itself or in combination with the partially-depleted (PD) SOI NMOS transistor 200. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively,

other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0084] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy device interface 920. The primary bus bridge 903 may also coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0085] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The

multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0086] The processing system 900 illustrated in Figure 24 is only an exemplary processing system with which the invention may be used. While Figure 24 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 a p+ gate FD SOI NMOS device 100, either by itself or in combination with the n+ gate PD SOI NMOS transistor 200. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0087] Although the present invention has been described with reference to a SOI substrate 40 (Figures 5-19) formed by a bonding and etching back method, it must be understood that the present invention is not limited to the above fabrication

method. Accordingly, other methods known in the art, for example, the ELTRAN process, may be also used, as desired.

[0088] Further, although the exemplary embodiments of the present invention have been described for only one fully-depleted (FD) SOI NMOS transistor 100 (Figures 5-19) formed in the memory array area, and for only one partially-depleted (PD) SOI NMOS transistor 200 (Figures 5-19) formed in the periphery area, it must be understood that the present invention contemplates the formation of a plurality of such MOSFET devices in their respective area of the same or different conductivity type.

[0089] The above description illustrates preferred embodiments that achieve the features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Modifications and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.